REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-23 are pending in the application. The Examiner additionally stated that claims 1-23 are rejected. By this amendment, claims 1, 9-10, 13-14, and 21-23 have been amended. Hence, claims 1-23 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §112

The Examiner rejected claims 10-21 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Examiner noted that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the Examiner pointed out that in each of independent claims 10 and 14, and consequently their dependent claims, applicants claim: "first program code for providing an instruction bus" and "second program code for providing a data bus". The Examiner noted that the only examples that can be thought of in which program code provides a bus is either in a simulation or when program code is used to drive chip fabrication, and that neither task is consistent with the scope of applicants' original disclosure.

Applicant has amended claims 10 and 14 to incorporate limitations that more specifically described the claimed invention. For example, both claims as amended recite that "program code" is used with a computing device, and that when the program code is used with the computing device, it causes enablement of functions corresponding to an

instruction bus or a data bus, as appropriate. Applicant notes in the specification that "[t]he program code causes the enablement of the functions or fabrication, or both, of the invention disclosed herein. For example, this can be accomplished through the use of general programming languages (e.g., C, C++, etc.), hardware description languages (HDL) including Verilog HDL, VHDL, AHDL (Altera Hardware Description Language) and so on, or other programming and/or circuit (i.e., schematic) capture tools available in the art." And furthermore, the specification notes that "[i]t is understood that the functions accomplished and/or structure provided by the invention as described above can be represented in a core that is embodied in program code and may be transformed to hardware as part of the production of integrated circuits. Also, the invention may be embodied as a combination of hardware and software."

In view of the above amendments to claims 10 and 14, and further in view of the noted descriptions drawn from the specification, Applicant respectfully submits that amended claims 10 and 14 contain subject matter which is described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention, and furthermore that the tasks recited are indeed consistent with the scope of the original disclosure.

Consequently, Applicant requests that the rejections of claims 10-21 be withdrawn.

The Examiner also rejected Claims 10-21 under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. The omitted elements noted are: how program code provides an instruction bus and a data bus.

As noted above, claims 10 and 14 have been amended to recite that "program code" is used with a computing device, and that when the program code is used with the computing device, it causes enablement of functions corresponding to an instruction bus or a data bus, as appropriate. Applicant therefore submits that the claim amendments bridge the noted gap by stating that the code is used with the computing device. Accordingly, it is requested that the rejections of claims 10-21 be withdrawn.

The Examiner furthermore rejected claims 9, 13, 21, and 23 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Referring to claims 9, 13, and 21, the Examiner stated that they claim transferring data in parallel to one or more coprocessors with multiple issue pipelines, and that it is unclear whether applicants are claiming transfer of multiple data elements (language of claim 1) in parallel or merely parallel data lines as opposed to a serial data line. Referring to claim 23, the Examiner noted that it is unclear as to how applicants designate "an execution order corresponding to said issuing." For example, the Examiner asked, if two or more instructions are issued at the same time to a coprocessor, how is the execution order of the two or more instructions determined, and how does it correspond to the parallel issue?

In response to the rejections, Applicant has amended claims 9, 13, 21, and 23 to recite "over parallel signal lines" in place of "in parallel," thus clearly denoting that the data (and instructions for the case of claim 23) is transferred over parallel signal lines to a coprocessor that has a multiple-issue execution pipeline. Claim 23 is also amended to recite "designating an execution order for the plurality of the instructions" which are issued over parallel signal lines, thus clarifying subject matter deemed to be the invention. Accordingly, it is requested that the rejections of claims 9, 13, 21, and 23 be withdrawn.

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1-9 and 22 under 35 U.S.C. 103(a) as being unpatentable over Coprocessor Interface (Chapter 10). Applicant respectfully traverses the rejections.

With reference to claim 1, the Examiner noted that Coprocessor Interface substantially taught the invention, including an interface for transferring data between a central processing unit (CPU) and a coprocessor, the interface comprising: an instruction bus, configured to transfer instructions to the coprocessor in an instruction transfer order, wherein particular instructions direct the coprocessor to transfer the data to/from the CPU (Sections 10.2 and 10.5.1, Fig. 10-1, and Table 10-2); and a data bus, coupled to said instruction bus, configured to transfer the data wherein data order signals within said data

bus specify a data transfer order that differs from said instruction transfer order, and wherein said data order signals specify transfer of a data element, said data element corresponding to a specific outstanding instruction wherein said data order is relative to outstanding instructions, said outstanding instructions being those of said particular instructions transferred to said the coprocessor that have not completed a data transfer; wherein the interface keeps track of said data order, and wherein said data order signals indicate said data order, and wherein said data order signals are provided with said data element as said data element is transferred (Sections 10.5.2 and 10.5.3 and Table 10-2, pp. 252 and 253).

The Examiner acknowledged that Coprocessor Interface did not teach interfacing with multiple coprocessors, though it did teach being able to interface with two types of coprocessors: a floating point processor and a graphics processor (Section 10.1, first paragraph). Thus, the examiner takes Official Notice of the facts that processors with multiple coprocessors were known in the art at the time of applicants' invention and that improvements in fabrication technology have made it possible to provide a processor and multiple coprocessors in the same amount of chip real estate once consumed by a processor and one coprocessor. The Examiner opined that one of ordinary skill in the art is motivated to provide a processor with multiple coprocessors to enhance performance through increased parallelism, and that one of ordinary skill in the art would be motivated to expand the capacity of the Coprocessor Interface to work with multiple coprocessors to provide a system with enhanced performance which permitted transfer of data and instructions in varying order thereby allowing greater flexibility in the use of system bus, etc. resources while still maintaining execution order.

Applicant agrees with the Examiner's statements that Coprocessor Interface did not teach interfacing with multiple coprocessors. But Applicant respectfully disagrees with the Examiner's further characterization of the cited reference and with the conclusions that are drawn based on the Official Notice. More specifically, Section 10.1, first paragraph is noted by the Examiner as teaching the ability to interface with two types of coprocessors: a floating point processor and a graphics processor. Very respectfully, Applicant asserts that this is not what is taught. The specific words of cited paragraph

state, "[t]he 5Kc coprocessor interface allows a ***single coprocessor,*** either Coprocessor 1 (COP1) ***or*** Coprocessor 2 (COP2), to be connected to the integer unit." COP1 is indeed taught to support floating point operations. But the reference states that COP2 is undefined. Regardless of the number of different *types* of coprocessors that are recited by the reference as being able for integration into the architecture, the reference clearly teaches that the interface supports only one processor.

Secondly, the cited reference is entirely silent with regard to providing an interface that supports multiple coprocessors, and that furthermore would support coprocessors having multiple issue execution pipelines. To take the teachings of the reference in combination with the Examiner's Official Notice, Applicant submits that one skilled in the art at the time of the invention would be motivated to replicate the coprocessor interface that is taught in order to interface to an additional processor. This is because the interface taught by the reference does not provide any means for designating or directing "one of a plurality of coprocessors," as is referred to in amended claims 1 and 22, to transfer data. The cited reference does not suggest, intimate, or even hint that multiple coprocessors can be interfaced in a manner such that instructions designate and direct one of the multiple coprocessor to transfer data.

Accordingly, it is respectfully requested that the rejections of amended claims 1 and 22 be withdrawn.

With respect to claims 2-9, these depend from claim 1 and add further limitations which are neither anticipated nor rendered obvious by Coprocessor Interface, the Examiner's Official Notice, or a combination thereof. It is therefore requested that the rejections of claims 2-9 be withdrawn as well.

Rejections Under 35 U.S.C. §101

The Examiner rejected claims 10-21 under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Applicant respectfully traverses the Examiner's rejections.

The Examiner noted that the computer program of claim 10 seems only to describe an interface, as in written description, and is not executed on a computer nor is it being

claimed as an element of a computer-related device. The Examiner furthermore pointed out that the computer program of claim 14 does not seem to be embodied in a tangible medium nor does the program seem to be executed.

In response, Applicant has amended claims 10 and 14 to recite that when the computer readable code is used with the computing device, it causes enablement of functions corresponding to a coprocessor interface. Applicant also respectively notes that the computer code of claim 14 is embodied within a transmission medium as a computer data signal. As the disclosure teaches, the transmission medium, allows for transmission of the computer code over communication networks including the Internet and intranets. As such, it is submitted that in order to transmit the computer code over communication networks via a transmission medium, it is required that the transmission medium be tangible.

In view of the above points, Applicant respectfully requests that the rejections of claims 10 and 14 be withdrawn.

Claims 11-13 and 15-21 depend from claims 10 and 14, respectively, and add further limitations beyond that which has been argued above as statutory subject matter. Accordingly, it is respectfully requested that the rejections of claims 11-13 and 15-21 be withdrawn as well.

CONCLUSIONS

In view of the arguments advanced above, Applicant respectfully submits that claims 1-23 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
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